AMENDMENTS TO THE CLAIMS:

1. (currently amended) An information processing device which reads, buffers, decodes, and executes instructions from an instruction store portion (11) by pipeline processing, comprising:

an instruction reading request portion (17) which assigns a read address to said instruction store portion;

an instruction buffering portion (12) including a plurality of instruction buffers (e-1, e-2) which buffer instruction sequences read from said instruction store portion;

an instruction execution unit ~~(29)~~ (20) which decodes and executes instructions buffered by said instruction buffering portion (12);

a branching instruction detection portion (14) which detects a branching instruction inside the instruction ~~sequence~~ sequences read from said instruction store portion; and

a branch target address information buffering portion (15) including at least first and second branch target address information buffers (b-1, b-2) which, when said branching instruction detection portion has detected a branching instruction, buffer ~~the~~ a branch target address information for generating a branch target address of said branching instruction;

wherein:

when said branching instruction detection portion (14) detects a first branching instruction (02) in a first instruction sequence being processed (C1) which is stored in one of said plurality of instruction buffers (e-1), a branch target instruction sequence (C2) of said first branching instruction (02) is stored in the other one of said plurality of instruction buffers (e-2), and said first instruction sequence (C1) and said branch target instruction sequence (C2) are fetched from said instruction store portion (11) and stored in said plurality of instruction buffers (e-1, e-2) sequentially,

when said branching instruction detection portion (14) detects a next branching instruction (04) following [[to]] the first branching instruction (02) in said first instruction sequence (C1), a first branch target address information (41) of the next branching instruction (04) is stored in the first branch target address information buffer (b-1) without prefetching a branch target instruction sequence of the next branching instruction,

when said branching instruction detection portion (14) detects a second branching instruction (12) in said branch target instruction sequence (C2), a second branch target address information (21) of the second branching instruction (12) is stored in the second branch target address information buffer (b-2) without prefetching a branch target instruction sequence of the second branching instruction, and

when said first branching instruction is executed, depending on the execution result of the first branching instruction, said branch target address information in either the first or second branch target address information buffer (b-1, b-2) is invalidated and another branch target instruction sequence starts to be fetched and stored in said instruction buffer, which is invalidated, based on the branch target address information which is not invalidated.

2. (currently amended) An information processing device which reads, buffers, decodes, and executes instructions from an instruction store portion by pipeline processing, comprising:

an instruction reading request portion which assigns a read address to said instruction store portion;

an instruction buffering portion including ~~a plurality of~~ first and second instruction buffers which buffer instruction sequences read from said instruction store portion;

an instruction execution unit which decodes and executes instructions buffered by said instruction buffering portion;

a branching instruction detection portion which detects a branching instruction inside the instruction sequences read from said instruction store portion; and

a branch target address information buffering portion including ~~a plurality of~~ first and second branch target address information buffers which, when said branching instruction detection portion has detected a branching instruction, buffer a branch target address information for generating a branch target address of said branching instruction;

wherein[[;]]:

a first instruction sequence (C1) being processed is stored in either one of the first or second instruction buffers (e-1) and when said branching instruction detection portion detects a branching instruction ~~(04)~~ (02) inside said first instruction sequence (C1), a second instruction sequence (C2) of the branch target of the branching instruction is stored in the other one of the first or second instruction buffers (e-2) in accordance with the branch target address information of said branching instruction (02);

the branch target address information (41) of a next branching instruction (04) inside said first instruction sequence (C1) ~~is stored in either one of the first instruction sequence (C1)~~ is stored in either one of the first or second branch target address information buffers (b-1) without prefetching a branch target instruction sequence of the next branching instruction (04); [[and]]

the branch target address information (21) of [[the]] a branching instruction (12) inside said second instruction sequence (C2) is stored in the other one of said first or second branch target address information buffers (b-2) without prefetching a branch target instruction sequence of the branching instruction (12); and

~~wherein~~ the first or second branch target address information buffer is selected based on an execution result of the branching instruction ~~(04)~~ (02) inside said first instruction sequence (C1).

3. (currently amended) The information processing device as claimed in Claim 2 wherein, in a state in which said first instruction sequence being ~~process~~ processed (C1) is stored in either one of said first or second instruction buffers (e-1), the second instruction sequence (C2) of the branch target of the branching instruction (02) inside said first instruction sequence is stored in the other one of said first or second instruction buffers (e-2), the branch target address information (41) of the next branching instruction (04) inside said first instruction sequence (C1) is stored in said first branch target address information buffer (b-1) and the branch target address information ~~(12)~~ (21) of the branching instruction (12) inside said second instruction sequence (C2) is stored in said second branching address information buffer (b-2);

if the execution of the branching instruction (02) inside said first instruction sequence (C1) has resulted in branching, said first instruction sequence (C1) and the branch target address information of the next branching instruction (04) inside said first instruction sequence (C1) are invalidated~~; and wherein~~ , a third instruction sequence (C4) of the branch target of the branching instruction (12) inside said second instruction sequence (C2) is stored in one of said first or second instruction buffers (e-1), in accordance with the branch target address information which ~~have~~ has been stored in the other one of said first or second branch target address information ~~buffer~~ buffers (b-2)[[;]] , and the branch target address information of the next branching instruction (14) inside said second instruction sequence (C2) is stored in one of the first or second branch target address information ~~buffer~~ buffers (b-1), and the branch target address

information of the branching instruction (22) inside said third instruction sequence (C4) is stored in the other one of said first or second branch target address information buffers (b-2).

4. (currently amended) The information processing device as claimed in claim 2 wherein, in a state in which said first instruction sequence being processed is stored in either one of said first or second instruction buffers, the second instruction sequence (C2) of ~~one of~~ the branch ~~targets~~ target of the branching instruction (02) inside said first instruction sequence (C1) is stored in the other one of said first or second instruction ~~buffer~~ buffers, the branch target address information of the next branching instruction (04) inside said first instruction sequence (C1) is stored in said first branch target address information buffer and the branch target address information of the branching instruction (12) inside said second instruction sequence (C2) is stored in said second branching address information buffer;

if the execution of the branching instruction (02) inside said first instruction sequence (C1) has not resulted in branching, said second instruction sequence (C2) and the branch target address information of the branching instruction (12) inside said second instruction sequence (C2) are invalidated;

~~the~~ fourth instruction sequence (C3) of the branch target of the next branching instruction (04) inside said first instruction sequence (C1) is stored in one of said first or second instruction ~~buffer~~ buffers, in accordance with the branch target address information which ~~have~~ has been stored in the other one of said first or second branch target address information ~~buffer~~ buffers; and

[[the]] branch target address information of [[the]] further next branching instruction inside said first instruction sequence (C1) is stored ~~again~~ in one of said first or second branch

target address information ~~buffer~~ buffers, and the branching address information of the branching instruction inside said fourth branching instruction sequence (C3) is stored in the other one of said first or second branch target address information buffers.

5. (original) The information processing device as claimed in claim 1 wherein, in response to a single instruction read request from said instruction reading request portion, a plurality of consecutive instructions from said read address are read from said instruction store portion and buffered in said instruction buffering portion.

6. (currently amended) An information processing device which reads, buffers, decodes and executes instructions from an instruction store portion by pipeline processing, comprising:

an instruction reading request portion which assigns a read address to said instruction store portion;

an instruction buffering portion including a plurality of instruction buffers which buffer instruction sequences read from said store portion;

an instruction execution unit which decodes and executes instructions buffered by said instruction buffering portion;

a branching instruction detection portion which detects a branching instruction inside the instruction ~~sequence~~ sequences read from said instruction store portion, and detects branching prediction information of the branching instruction; and

a branch target address information buffering portion including a plurality of branch target address information buffers which, when said instruction detection portion has detected a

branching instruction, buffers ~~buffer the~~ branch target address information for generating the branch target address of said branching instruction;

wherein:

when said branching instruction detection portion (14) detects a first branching instruction (02) in a first instruction sequence being processed (C1) which is stored in one of said plurality of instruction buffers (e-1), a branch target instruction sequence (C2) of said first branching instruction ~~(C2)~~ (02) is stored in the other one of said plurality of instruction buffers (e-2), and said first instruction sequence (C1) and said branch target instruction sequence (C2) are fetched from said instruction store portion (11) and stored in said plurality of instruction buffers (e-1, e-2) sequentially,

when said branching instruction detection portion (14) detects a next branching instruction (04) following [[to]] the first branching instruction (02) in said first instruction sequence (C1), a first branch target address information (41) of the next branching instruction (04) is stored in the first branch target address information buffer (b-1) without prefetching a branch target instruction sequence of the next branching instructions,

when said branching instruction detection portion (14) detects a second branching instruction (12) in said branch target instruction sequence (C2), a second branch target address information (21) of the second branching instruction (12) is stored in the second branch target address information buffer (b-2) without prefetching a branch target instruction sequence of the second branching instructions, and

when said first branching instruction is executed, depending on the execution result of the first branching instruction, said branch target address information in either the first or second branch target address information buffer (b-1, b-2) is invalidated and another branch target

instruction sequence starts to be fetched and stored in said instruction buffer, which is invalidated, based on the branch target address information which is not invalidated.

7. (currently amended) The information processing device as claimed in claim 6 wherein, whether ~~aid~~ said branch target address information buffering portion buffers the branch target address information of a branching instruction is determined in accordance with the branching prediction information of said branching instruction which is detected by said instruction detection portion.

8. (currently amended) The information processing device as claimed in claim 6 wherein, whether said instruction buffering portion fetches the branch target instruction sequence of said branching instruction is determined in accordance with [[a]] the branching prediction information of the branching instruction which is detected by said instruction detection portion.

9. (currently amended) The information processing device as claimed in claim 6 wherein, if said branching instruction detection portion predicts with a prescribed high level of probability that [[a]] the branching instruction will not branch, said branch target address information buffering portion does not fetch the branch target instruction ~~sequenced~~ sequence of said branching instruction.

10. (original) The information processing device as claimed in claim 6 wherein, when said branch target address information buffering portion has buffered branch target address information of a first branching instruction, if said branching instruction detection portion has

detected a second branching instruction which has a greater possibility of branching than said first branching instruction, said branch target address information buffering portion invalidates the branch target address information of said first branching instruction and buffers the branch target address information of said second branching instruction.

11. (previously presented) The information processing device as claimed in claim 6 wherein, when one of said instruction buffers of said instruction buffering portion is empty, if a first branching instruction having a first branching possibility is detected by said branching instruction detection portion, a branch target instruction sequence of said first branching instruction is not fetched to said instruction buffering portion and said branching target address information buffering portion buffers the branch target address information of the first branching instruction, and if said branching instruction detection portion has detected a second branching instruction which has a second branching possibility which is higher than said first branching possibility, a branch target instruction sequence of said second branching instruction is fetched to said instruction buffering portion.

12. (previously presented) An information processing device with a pipeline processing comprising:

an instruction fetch portion which fetches both a sequential side instruction sequence and a target side instruction sequence of a branching instruction in spite of a branching prediction of the branching instruction;

a cache controller which fetches instructions from a cache memory or from a main memory in response to a fetch request from said instruction fetch portion;

a memory bus access portion which accesses said main memory;

an instruction buffer which buffers instructions which have been fetched; and

a branching prediction portion which, prior to an execution of a branching instruction, performs a branching prediction for the branching instruction which is stored in said instruction buffer;

wherein, if a branching direction of said branching instruction is not yet determined, said cache controller performs a memory bus access to said main memory according to a branching direction predicted by the branching prediction portion.

13. (previously presented) The information processing device as claimed in claim 12 wherein, while the branching direction of said branching instruction is not yet determined, if the cache controller has performed a cache miss with respect to an instruction in the predicted branching direction of said branching instruction, said cache controller performs the memory bus access to the main memory for an instruction fetch, and if said cache controller has performed a cache miss with respect to an instruction which is not in the predicted branching direction, said cache controller does not perform the memory bus access and stops the instruction fetch.

14. (currently amended) The information processing device as claimed in claim 12 wherein, while the branching direction of said branching instruction is not yet determined [[an]] and the predicted branching direction of said branching instruction is the sequential side, in the event of said cache controller performing a cache miss with respect to said target side instruction, said cache controller does not perform a memory bus access and stops the instruction fetch.

15. (currently amended) The information processing device as claimed in claim 12 wherein, while the branching direction of said branching instruction is not yet determined, said cache controller does not perform a memory bus access after a cache miss depending on [[eh]] the predicted branching direction of said branching instruction.

16. (currently amended) An information processing device ~~with a pipeline processing~~, comprising:

an instruction fetch portion which fetches both a sequential side instruction ~~sequences~~ sequence and a target side instruction ~~sequences~~ sequence of a branching instruction in spite of a branching prediction of the branching instruction;

a cache controller which fetches instructions from a cache memory or from a main memory in response to a fetch request from said instruction fetch portion;

a memory bus access portion which accesses said main memory;

an instruction buffer which buffers instructions which have been fetched; and

a branching prediction portion which, prior to an execution of a branching instruction, performs a branching prediction of the branching instruction which is stored in said instruction buffer;

wherein, if a branching direction of said branching instruction is not yet determined and said cache controller performs a cache miss with respect to an instruction fetch, said cache controller does not perform a memory bus access and stops ~~the~~ said instruction fetch, and if said branching direction of said branching instruction has been determined and said cache controller performs a cache miss with respect to an instruction in the determined branching direction, said cache controller performs a memory bus access.

17. (original) The information processing device as claimed in claim 16 wherein, if the branching direction of said branching instruction is not yet determined, an instruction for which a cache hit has been made is prefetched and stored in said instruction buffer.

18. (currently amended) The information processing device as claimed in claim 16 wherein, instructions are selected from either said sequential side instruction sequence [[of]] or target side instruction sequence in said instruction buffer depending on the branching direction of the branching prediction portion, and decoded.